

REMARKS/ARGUMENTS

Claims 1-6, 8-21, and 23-27 are pending in the present application, Applicants having cancelled claims 7 and 22 in the previous response.

In the Office Action, the Examiner has maintained the rejection of claims 1-4, 8, 9, 13-19, 23, 24 under 35 U.S.C. §102(e) as anticipated by Au. The Examiner also has maintained the rejections of claims 5, 10-12, 20, and 25-27 under 35 U.S.C. §103(a) as unpatentable over Au in view of USP 6,370,661 (Miner), and of claims 6 and 21 under 35 U.S.C. § 103(a) as unpatentable over Au and further in view of USP 7,010,736 (Teh). Applicants respectfully traverse these rejections, and submit that the rejections are overcome further by the foregoing amendments to the claims. Applicants request reconsideration and allowance of the claims in view of the following arguments.

As Applicants discussed in the previous response, the present invention relates to a memory testing method and system in which memory testing is conducted at the operating frequency of the memory until an error is identified. By testing at the memory operating frequency, as Applicants describe, errors which can occur at otherwise more rapid speeds can be identified. Importantly, if a failed memory location is identified, *the location information for that failure is identified at the memory operating frequency*, and is clocked out to a memory tester at a lower, tester frequency.

The Examiner has maintained that the Au reference teaches testing at two different speeds. However, what Au clearly fails to teach or suggest, and which Miner likewise fails to teach or suggest, is the identification of failure location information at the higher speed. On page 2 of the Office Action, the Examiner says that Au teaches that “[i]f a failure is identified, the

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location information is clocked out to a memory tester (the ATE referred to throughout the disclosure) at a lower, tester frequency.” Assuming for the sake of argument that the Examiner’s characterization of Au is correct, nevertheless, all Au teaches is the identification of the **existence** of an error through a first pass test at the higher speed. Nowhere does Au teach or suggest *the identification of failure location information at the higher speed*. In order for Au to detect failure location information, Au must test again at a **lower** speed, not at the higher speed.

Au’s first pass test identifies that there is a failure in the memory under test. However, Au’s first pass test does not identify *where* the failure is. That location identification is left to the second pass test, which occurs at a **slower** speed.

As Applicants also discussed in the last response, according to the present invention, memory testing is initiated at a higher speed, which (as recited in dependent claims, but not claims 1, 13, or 16) is the memory operating frequency. **If an error is detected, failure location information is identified at that higher speed (the first frequency)**, and is clocked out at a lower, tester frequency (second frequency). Testing is then resumed at the higher frequency.

Au describes a non-debug mode of operation in which a memory is tested at the memory operating frequency, and errors are counted. *See, e.g.*, col. 5, lines 26-30; col. 7, lines 63-65. At the end of the test, the count is output. **This test does not identify errors by memory location.** This test **only** provides a count. In order to identify errors by memory location, Au must conduct a second test at a slower speed, in a debug mode of operation, in which memory testing is carried out at a lower frequency. *See, e.g.*, col. 5, lines 30-32; col. 7, line 66 to col. 8, line 3.

The Au system selects either the debug test mode **or** the nondebug test mode based on a two-bit mode selection register. *See* col. 7, lines 53-61.

Au also describes testing as preferably beginning in a faster, non-debug mode (col. 8, lines 56-58). Testing in this mode is performed at the full operational speed of the memory, and **results in a simple pass/fail verdict, together with a failure count** (col. 8, lines 59-61).

From col. 8, line 56 to col. 9, line 24, Au describes its two different DEBUG and NONDEBUG modes of testing. Au also provides flow charts for both modes of operation, describing the NONDEBUG mode with reference to the Fig. 4 flow chart, and the DEBUG mode with reference to the Fig. 5 flow chart. The Fig. 4 flow chart, corresponding to the faster NONDEBUG mode test, clearly shows scanning out a failure count (step 166), but Fig. 4 and the accompanying description say nothing about failure location information. The Fig. 5 flow chart, corresponding to the slower DEBUG mode test, shows scanning out failure information (step 188) which comprises a 100-bit packet including failed cell location (col. 10, lines 39-42).

In order for a prior art reference to anticipate a claim, it must disclose, expressly or under principles of inherency, all of the claimed limitations. Applicants respectfully submit that Au fails to anticipate or render obvious the claims of the present application because Au does not disclose or suggest **c** (first frequency), as recited in independent claims 1, 13, or 16, and hence in their dependencies. Neither Miner nor Teh, which the Examiner has applied against dependent claims, remedy any of the deficiencies of Au. Therefore, pursuant to the foregoing discussion, Applicants respectfully request that the Examiner reconsider and withdraw these rejections, and submit that claims 1-6, 8-21, and 23-27 are patentable..

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Request for Allowance

It is believed that this Amendment places the application in condition for allowance, and early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,
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